



Zirconium Oxide Mixed Tantalum Oxide High-K Gate Dielectric Films for Metal-Oxide-Semiconductor (MOS) Devices

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ABSTRACT

Hafnium oxide mixed tantalum oxide (HTO) and Zirconium oxide mixed tantalum oxide (ZTO) layers were deposited on chemically cleaned p-Si substrate using RF magnetron sputtering technique. The oxide/Si stacks were annealed in oxygen for 30 minutes at 400 °C as on initial investigation. Both composition and structural properties were absolutely interesting to move further for electrical measurements. In continuation, metal-oxide-semiconductor devices were fabricated with aluminum gate electrode. ZTO devices showed attractive dielectric and electrical properties, relatively when compare with HTO devices, it could be due to the electrical, chemical and thermal properties of ZTO layer with Si, resulting good interface at ZTO/Si stack.

Key words: Metal-Oxide-Semiconductor (MOS) Devices, HTO, ZTO, High-K Gate Dielectric Films

INTRODUCTION

As Integrated circuitry (IC) technology becomes more and more advance, more semiconductor devices get stuffed in to small spaces. Smaller device size enables higher device density in an integrated circuit, resulting improvement device performance [1]. The significant reduction in size of silicon devices directly associated to the reduction in size of gate oxide such as silicon oxide (SiO₂) layer thickness, (< 2 nm). This leads to higher leakage currents and worsen the device performance [2]. The scaling of equivalent oxide thickness (EOT) represents the most important issue in the development of complementary-metal-oxide-semiconductor devices. Compared to SiO₂, transition metal-oxides with high dielectric constant (high-k) have the enormous advantage of EOT scaling with a lower leakage currents.[3-4] Among the various mono high-k materials, such as tantalum oxide (Ta₂O₅), zirconium oxide (ZrO₂), hafnium oxide (HfO₂) and titanium oxide (TiO₂), tantalum oxide has been widely studied both experimentally and theoretically over the past three decades, due to its potential application in dynamic random access memory (DRAM), and sensors[5-8], whereas the thermodynamic instability of Ta₂O₅ with Si, reduces the effective dielectric constant [9-10]. The quite small electron barrier height with the Si conduction band exacerbates the device leakage [11-12]. On the other hand many investigations were made on (ZrO₂) as a high-k gate dielectric layer for next generation MOSFET devices [13-16]. The ZrO₂ also has a high dielectric constant (~24), a wide band gap (~5.8 eV), and has a good thermodynamic stability with Si [17]. But ZrO₂ has low amorphous-to-polycrystalline transition temperature, which is definitely too low for ULSI processing [18]. Besides HfO₂ is also a promising candidate for the next generation of gate dielectrics due to its high free energy of reaction with Si substrate, apart from its regular dielectric properties [19-20]. However, HfO₂ severely struggling with the large oxygen vacancies. It is possible to overcome all the above said defects of mono high-k layers either by doping dopants or by mixing different high-k materials to improve the structural and electrical properties for various applications [21-22] and dissipation factor were found to be improved with an optimized doping concentration. Salam et al. studied the doping effect on thin Ta₂O₅ films and claimed that the mixing of TiO₂ or WO₃ with Ta₂O₅ improved several

dielectric and insulating properties [23]. In order to obtain better insulating properties, it was prepared in multilayer structures with Al_2O_3 , HfO_2 , or ZrO_2 [8, 24-25]. The best dielectric properties were obtained with a zirconium doped/mixed tantalum oxide film, other dopant Ti was found to increase the dielectric constant drastically [26-28]. However, the amorphous-to-crystalline transition temperature as well as leakage currents were degraded by the Ti doping. A low-quality interface layer was also observed between the Ti-doped TaOx film and the Si substrate. Many electrical properties, such as dielectric constant, leakage current, flat band shift, and hysteresis, showed great improvement with the Hf doping tantalum oxide [29-30]. Among all the dopants, Zr was the only one that was beneficial for dielectric constant enhancement. Without disturbing the interface at oxide/Si interface so it might a promising candidate for the next generation gate dielectric layer for the MOS device with high dielectric constant (~28), wide band gap, good thermal stability and high amorphous to polycrystalline transition temperature. Hence in this investigation we studied the structural and electrical properties of Zirconium oxide mixed tantalum oxide (ZTO) and Hafnium oxide mixed tantalum oxide (HTO) MOS devices with Al electrode and compare them. ZTO MOS device showed relatively better electrical properties when compare with the HTO MOS devices due to their chemical, electrical and thermal properties.

EXPERIMENTAL DETAILS

After removing the native oxide on p-type Si <100> wafers with doping concentration of Si $5 \times 10^{15} \text{ cm}^{-3}$, 24 nm thick ZTO and HTO layers were deposited on chemically cleaned p-type Si <100> wafers, using rf magnetron co-sputtering technique from 99% pure ZrO_2 , HfO_2 and Ta_2O_5 ceramic targets. Pre-sputtering step was done for 10 minutes with pure Ar to clean the target surface. The deposition pressure was 0.3 pa with an Ar/ O_2 ratio of 14/1 sccm without any intentional substrate heating to avoid influences the film's conformity and topology. The dielectric film thickness was measured with an ellipsometer (Rudolph i1000). The ZTO/Si and HTO/Si stacks were annealed at 400 °C for 30 minutes in oxygen (O_2) rich environment. After annealing, wafer's backside was etched with a buffered HF solution in order to remove the SiO_2 film prior to the deposition of Al film as the back contact by using electron beam evaporation technique. Rutherford back scattering (RBS), technique was used for the chemical bonding and elemental composition analysis. The crystallographic structure of the annealed ZTO and HTO layers was analyzed with X-ray diffractometer (XRD), For a gate electrode, 50 nm thick Al film with dimensions $1 \times 1 \text{ mm}^2$ was deposited using shadow mask. The interface quality and dielectric constant of the mixed high-k layers were extracted by capacitance-voltage (C-V) curves obtained from Al/ZTO/Si and Al/HTO/Si stacks. The C-V characteristics were measured at different frequencies, eg. 10,100 and 1000 KHZ at room temperature using a multi frequency LCR meter (HP impedance analyzer (4284A)). These C-V curves are imposed or fitted into the quantum mechanical simulation by using the MathCAD software then we obtain the equivalent oxide thickness and flat band voltage. Current- voltage (I-V) characteristics were determined using a precision semiconductor analyzer (Agilent 4156C).

RESULT AND DISCUSSION

The energy barriers (indicated by arrows in the figure) are corresponding to the energy of the detected particles that have been backscattered by Ta, Hf/Zr and O surface atoms of the sputtered film. In the case of the Ta:Hf:O film, the Hf barrier is overlapped with the energy of particles backscattered by Ta atoms. In both samples, the O contribution is superimposed on the Si/ SiO_2 substrate. As can be seen in the figures, the film composition is revealed by the different Ta and Hf (or Zr) barrier yield heights. Analysis with NDF program was made to extract the film's composition that best describes each sample. Our previous studies have revealed that thermal annealing condition have the significant effect on the change occurred in crystallographic structure and electrical properties of sputtered Ta_2O_5 [31], TiO_2 [32] and atomic layer deposited HfO_2 [33] layers. These noticeable structural changes in the gate oxide may possible associated with the electrical properties of that particular oxide's MOS devices. To know the effect of thermal treatment on the structural properties of ZTO and HTO layers we carried out the XRD measurement (Fig.2). It is clear from the spectra that, no diffraction peak was observed in both annealed oxide layers. It seems that both ZTO and HTO layers were amorphous in nature. In general, polycrystalline form of a gate dielectric is not preferred for transistor applications. It is quite interesting to have an amorphous high-k layer after thermal treatment to achieve reliable electrical properties with low leakage currents. This occurs because the dopant atoms distort the originally more ordered structure and thus increase entropy, which suppresses the crystallization process [34]. Hence, we also observed amorphous ZTO and HTO layers after annealing, may be due to the mixing of Ta_2O_5 with ZrO_2 and HfO_2 .

Fig.3 shows the C-V characteristics of the MOS device with different frequencies measured on as-deposited ZTO and HTO MOS devices before annealing process. It is clear from Fig. 3(a) particularly, the accumulation region was relatively stable and there was no large frequency dispersion in the device. Besides, there was much difference in the as-deposited C-V curves of HTO device fig. 3(b) that the accumulation region was highly unstable and huge frequency dispersion in accumulation and inversion regions; it might be due to the low interface quality and high

series resistance in the stacks [35]. Resulting that the ZTO device might have relatively good interface at ZTO/Si stacks, when compare with HTO/Si stacks. It could be owing to the chemical reactions in between HTO/Si and ZTO/Si stacks [35-36].

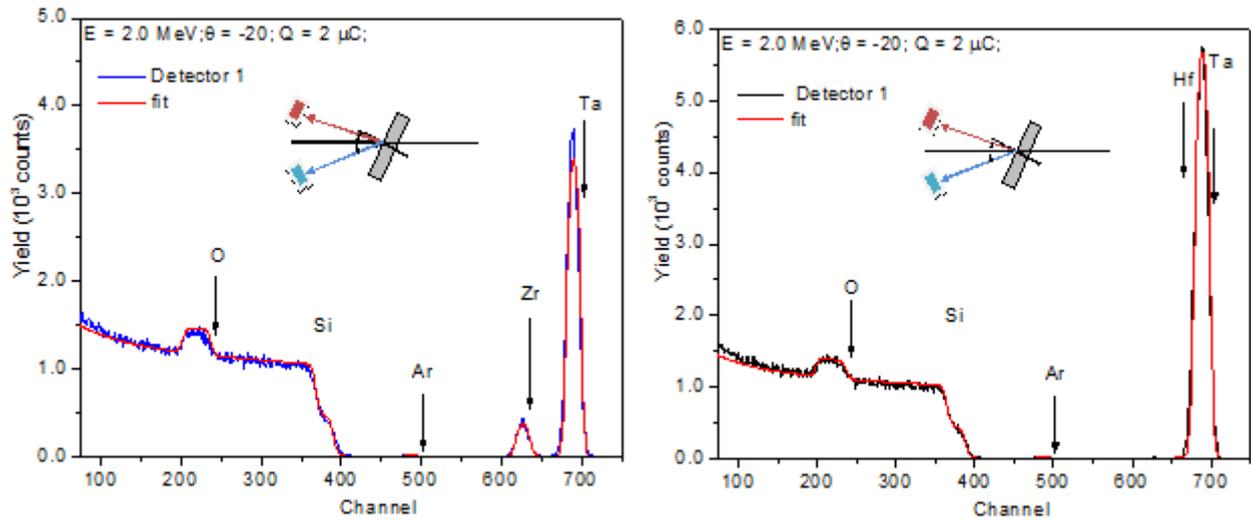


Fig. 1 RBS spectra of (left) Ta:Zr:O film and (right) Ta:Hf:O with fitted spectra

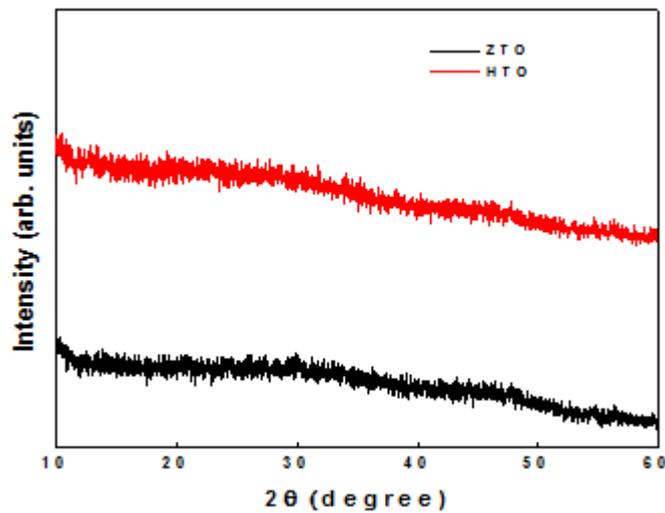


Fig. 2 X-ray diffraction spectrum of annealed ZTO and HTO layers

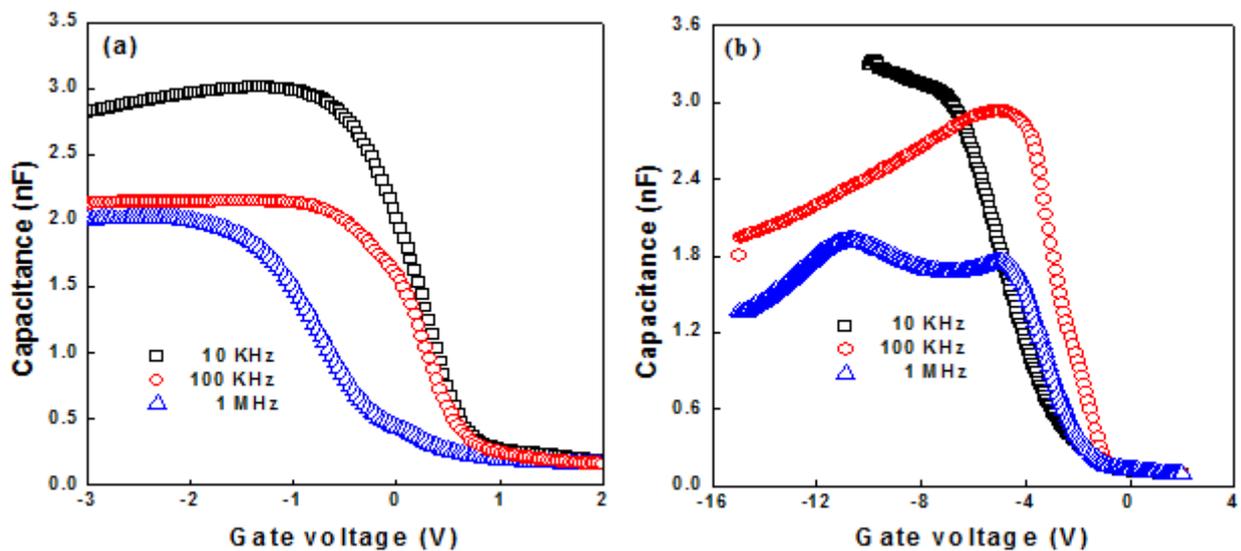


Fig. 3 Capacitance-voltage characteristics of as-deposited (a) ZTO and (b) HTO devices

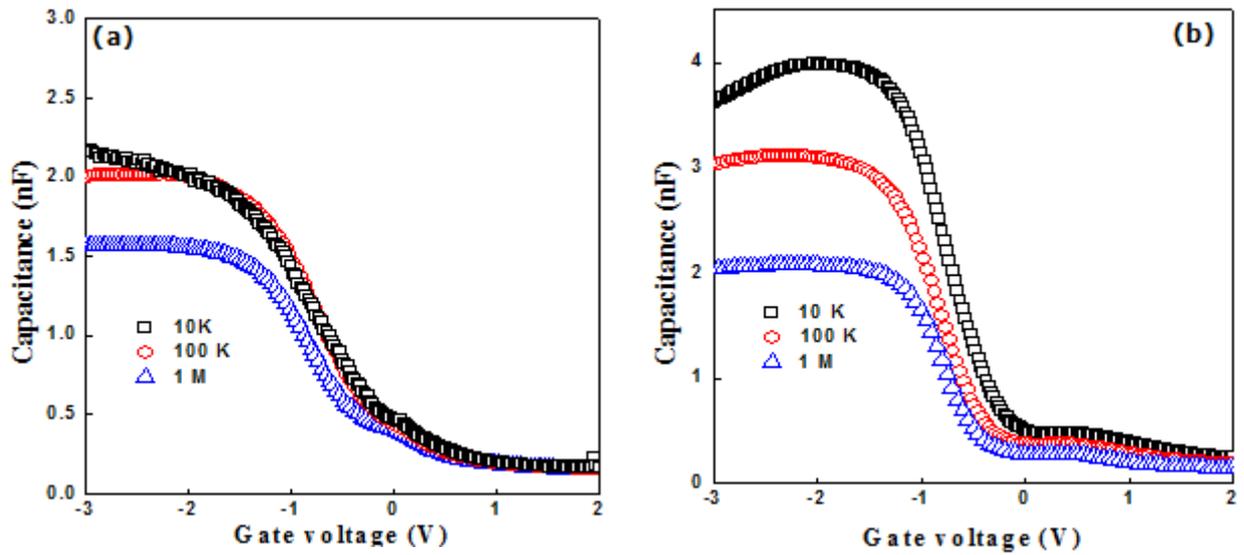


Fig. 4 Capacitance-voltage characteristics of annealed (a) ZTO and (b) HTO devices

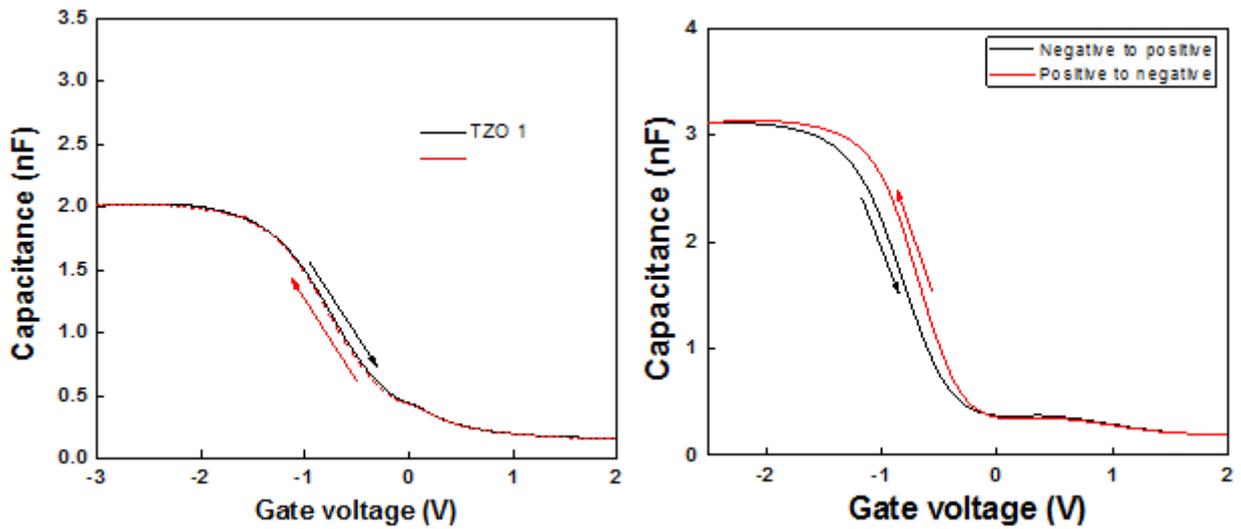


Fig. 5 Hysteresis curves of annealed (a) ZTO and (b) HTO devices

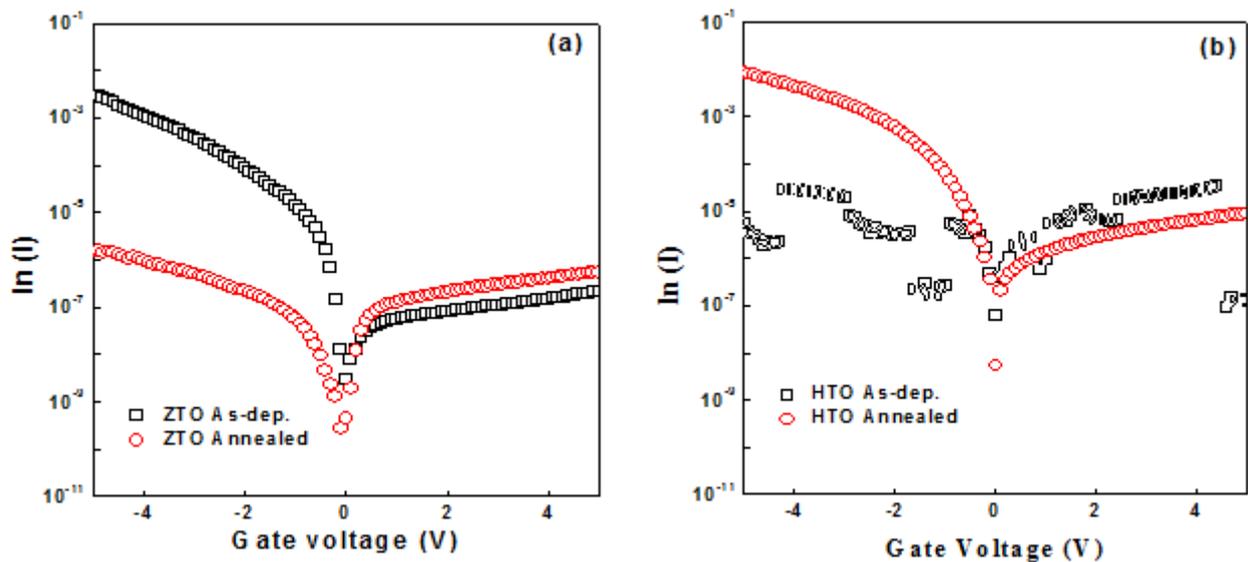


Fig. 6 Current-voltage curves of (a) ZTO and (b) HTO devices

Fig.4 shows the C-V characteristics of the MOS device with different frequencies measured on annealed ZTO and HTO MOS devices. The C-V curves obtained on ZTO device; [fig 4(a)] showed stable in accumulation region and low frequency dispersion at accumulation, depletion and inversion regions. It is clear from the HTO devices, there was instability in the accumulation region shown in [Fig. 4(b)] with a noticeable kink in the inversion region. These two observations are the direct significance for the large frequency dispersion and low quality of the device with high density of interface trap states (D_{it}) and high leakage currents. On the other hand, there were much noticeable frequency dispersions in the accumulation and depletion regions of the HTO device; it could be due to the influence of series resistance in the device. It might be happened owing to the presence of significant oxygen vacancies and the chemical interaction between the Si substrate and plasma (Hf:Ta:O) present in the sputter chamber, eventually forms hafnium silicates at the interface of HTO/Si stacks during deposition. Whereas, ZTO devices showed good interface quality and less influence of series resistance in ZTO device when compare with HTO device. It means that there was less possibility of forming zirconium silicates at ZTO/Si stacks during the process of annealing. It might be due to the good thermal interaction of ZrO_2 and Ta_2O_5 with Si substrate and less oxygen vacancies in ZTO layer. It seems that these two ZrO_2 and Ta_2O_5 may have relatively good interaction with Si substrate [36-37].

To confirm the quality of ZTO/Si and HTO/Si stacks bulk and interface regions, we extract hysteresis curves from annealed ZTO and HTO devices. Fig. 5 shows the hysteresis curves drawn by varying applying voltage from -3 to +2V. There was almost no hysteresis in ZTO layers [Fig.5 (a)]; it seems that the ZTO/Si stacks are not suffering much with presence of high density of interface state defect (D_{it}), oxygen vacancies and bulk defects in ZTO layers after O_2 annealing. On the other hand, there was noticeable large hysteresis voltage in HTO layers [Fig 5(b)]. The bulk defect density and the presence of oxygen vacancies in HTO layer might be the plausible reason for this observation. The believable reason for these bulk defects in HTO layer would be the presence of hafnium atoms in the high-k layer, since HfO_2 severely struggling with oxygen vacancies [38].

The current-voltage characteristics were shown in fig. 6. It is clear from the I-V plots that the leakage current in ZTO devices [Fig.6(a)] are relatively low when compare with HTO devices [Fig.6(b)] before and after annealing process. For instance the leakage current at around 0.5 V for ZTO devices before the annealing process was $\sim 7.1 \times 10^{-8}$ Amp, and it has to be reduced to $\sim 3.5 \times 10^{-8}$ Amp, after annealing. Whereas, for HTO device the leakage currents noticed at 0.5 V were $\sim 1.8 \times 10^{-6}$ and 7.1×10^{-7} Amp, before and after annealing, respectively. The reason for this observation could be the poor interface by formation of hafnium silicates at HTO/Si interface, transported oxygen vacancies from the bulk oxide and high bulk defect density as explained above.

CONCLUSION

Deposition of new high-k gate dielectric by mixing of Ta_2O_5 with ZrO_2 and HfO_2 using co-sputtering technique, require thermodynamic stability, high range of amorphous-to-crystalline transition temperature, a large electrical bandgap, and a large energy band barrier with Si. A new high-k gate dielectric material, i.e., ZTO device was proposed to improve the structural and electrical properties when comparing with HTO device. The new ZTO/Si stacked structure showed several advantages, such as a higher dielectric constant, a lower leakage current, and a higher breakdown field over HTO/Si stacks. XRD spectrum revealed that the transition temperature from amorphous-to-crystalline increased to $\sim 500^\circ C$ in the case of ZTO devices. The dielectric constant was increased from 14 to 27 for the ZTO devices with annealing. It could be due to the structural variations in the Zirconium oxide layer. The interface quality was also improved in ZTO devices with annealing by reducing the D_{it} level from 8×10^{11} to $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. Besides, the leakage current density is also reduced from the range of 10^{-7} to 10^{-9} A/cm^2 with respect to annealing process. All the above properties were worsen in HTO devices, relatively when compare with ZTO devices. Therefore, the ZTO device is a promising candidate for the future high-k gate dielectric applications comparing with HTO device.

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