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Effect of Substrate Material on the Electrical Properties of HfO_2 MOS Device

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ABSTRACT

Hafnium oxide (HfO_2) films were grown by atomic layer deposition on chemically cleaned p-type Ge and Si substrates with different thicknesses. For the electrical measurements, we fabricated the metal-oxide-semiconductor (MOS) devices with Platinum (Pt) electrode. The capacitance-voltage and current-voltage characteristics were measured on the sandwich structure of Pt/HfO_2/substrate. From the C-V measurement and we confirmed that the accumulation capacitance is reduced more significantly in the Si device than Ge device, might be thickness of interfacial layer (IL) at the HfO_2/semiconductor. The Ge device exhibited thin interfacial layers than Si device and it is thermally unstable. The measured dielectric constant value is relative high for Ge-devices when compare with Si-devices. Besides, Ge device exhibited similar leakage current as Si devices. Therefore, Ge might be a reliable substrate material for high frequency MOS devices.

Key words: Hafnium oxide films, metal-oxide-semiconductor Bras, capacitance-voltage and current-voltage characteristics

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INTRODUCTION

The most electronic systems are built on the integrated circuits (IC), which is an ensemble of both active (e.g., transistor) and passive (e.g., resistors, capacitors, and inductor) devices formed on and within a single-crystal semiconductor substrate and interconnected by a metallization pattern [1]. The minimum device dimensions, also called the minimum feature length. According to the International Technology Roadmap for Semiconductor, the minimum feature length will shrink from 130nm (0.13µm) in the year of 2002 to 35 nm (0.03µm) around 2014 [2]. The smaller device size enables higher device density in an integrated circuit, resulting improvement device performance and drastic reduction in processing cost [3]. As the gate length shrinks below 130nm, the oxide equivalent thickness of the gate dielectric must be reduced around 2nm to maintain permanence. However, if only SiO_2 (with dielectric constant of 3.9) is used, the leakage through the gate becomes very high and worsens the device performance because of direct tunnelling [4]. The scaling of equivalent oxide thickness (EOT) represents the most important issue in the development of complementary-metal-oxide-semiconductor devices. Compared to SiO_2, transition metal-oxides with high dielectric constant (high-k) have the enormous advantage of EOT scaling with a lower leakage currents [5-6]. For this reason various mono high-k materials, such as hafnium oxide (HfO_2), (~25), tantalum oxide (Ta_2O_5), (25), zirconium oxide (ZrO_2), (24), titanium oxide (TiO_2), (60-100) and silicon nitride (Si_3N_4), (~7) [7-10].

Among the various high-k materials, hafnium oxide (HfO_2) is a promising candidate for the next generation of gate dielectric due to its high dielectric constant (~25), wide band gap, good thermal stability, and relatively high free energy of reaction with Si substrate [11-12]. Recently, Ge based electronic devices regained considerable attention. Ge can provide solutions for major problems that Si technology facing for advanced CMOS devices; this is mainly due to higher mobility-of both electrons and holes in Ge substrate [13]. The benefits of employing high-k gate dielectrics on Ge include a thin interfacial layer (IL) between the high-k material and the Ge, and the possibility of hiding the imperfect properties of native oxide in capacitance scaling [14-15]. This implies that there are many

chances for us to challenge the integration of a Ge channel and high-k gate dielectric with a negligible effect on low-permittivity IL. Previously, Chui et al [16] demonstrated the device performance of functional Ge metal-oxide-semiconductor field-effect transistors (MOSFET) with high-k gate dielectrics. They also showed the possibility of enhancing the high frequency performance of digital logic devices by taking advantage of the higher carrier mobilises in Ge. Chen et al [17] obtained reasonably low EOT values for HfO_2/Ge stacks with good electrical properties. Kita et al [18] obtained a direct interface without an interfacial layer at the interface in between the high-k gate dielectric and Ge substrate. This is quite different from the interface of a Si/high-k gate stack. The band gap is an important parameter of a semiconductor material, because it affects the supply voltage and the scalability of a device. The germanium band gap (Eg Æ 0.66 eV) is significantly smaller than the silicon band gap (Eg Æ 1.12 eV), but still large enough to avoid instabilities through thermionic emissions and band-to-band tunneling [19]. Moreover, the lower band gap makes it possible to operate devices at lower voltages [20]. This reduces the power consumption, making it interesting especially for the growing market of mobile devices. Another advantage is that germanium requires lower temperatures for dopant activation which might allow for an easier integration with a high-k dielectric material like HfO_2 [20]. In this study, electrical and structural properties of Ge and Si metal-oxide-semiconductor (MOS) devices with Pt electrode on HfO_2 were investigated. Pt has a relatively high vacuum work function ($\phi_{m,vac}$) of 5.56eV [21].

EXPERMENTAL DETAIL

The p-type Ge (100) and p-type Si (100) wafers with doping concentration of $5x10^{15}$ cm^{-3} were used in this study. After removing the native oxide,HfO_2 film thickness of 6.0, 8.0, and 10.0nm were grown on the wafers using the atomic layer deposition process with $HfCl_4$ and H_2O sources at a wafer temperature of 300°C. The physical thicknesses of the HfO_2 films were determined using Ellipsometry measurements. For a gate electrode, 50nm thick Pt films were sputter-deposited at room temperature. After gate patterning with dimensions of 300 µm ×300 µm using lift-off lithography. Capacitance-Voltage (C-V) and conductance-voltage (G-V) characteristics were measured at 1MHz by HP4284A Precision LCR meter. The I-V characterizations were performed using HP 4156 parameter analyzer. All values of EOT and flatland voltages (V_{FB}) were determined by fitting the measured C-V curves with quantum mechanical simulation curves.

RESULT AND DISCUSSION

Fig. 1 shows the C-V characteristics of the Ge and Si MOS device with different frequencies with 10.0 nm thick HfO_2 as-deposited gate dielectric films. The C-V measurements at 1 and 10 KHZ demonstrate negligible frequency dispersion, implying an insignificant effect of series resistance on C-V characteristics. It is clear from the [fig 1. (a)] the frequency dispersion in the accumulation region is due to the substrate series resistance Rs, which is mainly effect to the high frequency C-V curves, kinks seen in the inversion regions at high frequency implying the existence of fast surface states near the valance band E_v. the difference between the 10 and 100 KHZ C-V curves in the same region indicates the presence of slow interface states as well [22]. In besides it is clear from fig 1.(b) shows there is negligible frequency dispersion at Appling different frequencies. From the C-V measurement and we confirmed that the accumulation capacitance is reduced more significantly in the Si device than Ge device, this could be attributed to the relatively large increase in the thickness of the interfacial oxide between HfO_2 and the Si substrate.

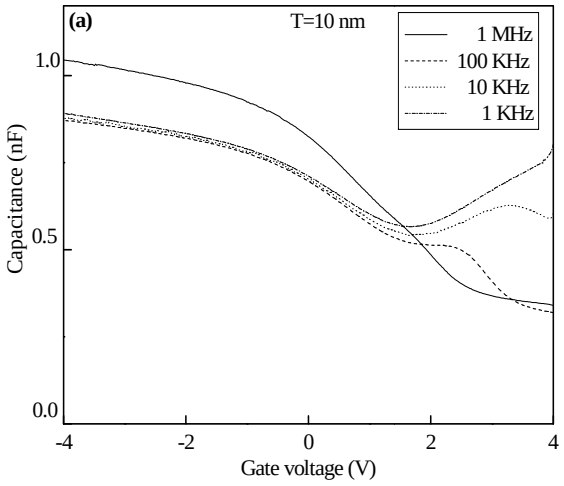

Fig. 1(a)

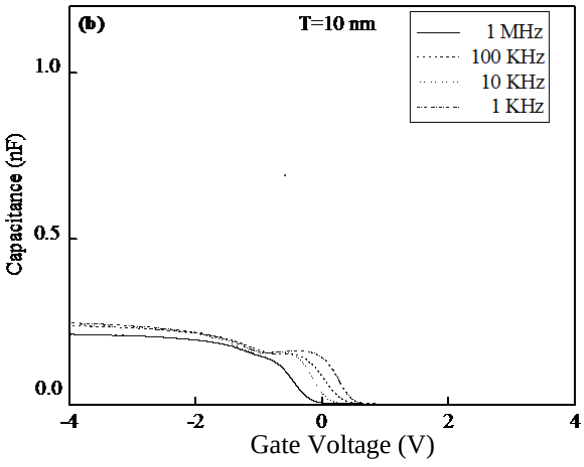

Fig. 1(b)

Fig. 1 Capacitance – voltage characteristics of (a) Ge- (b) Si- MOS devices at different frequencies

Fig. 2 Shows the C-V characteristics of the Ge and Si MOS devices applied at 1MHZ frequencies with 6.0, 8.0 and 10.0 nm thick HfO_2 as-deposited gate dielectric films. In the [fig 2(a)] C-V curves are not clear at accumulation, depletion and inversion regions, it could resulting to HfO_2 interfacial quality, such as D_{it} related Ge dangling bond at the substrate/gate dielectric interface. in besides it is clear [from fig 2(b)] C-V curves are clear at accumulation, depletion and inversions regions, from the C-V measurements we confirmed that the accumulation capacitance is reduced more significantly in the Si device than Ge device. This could be attributed to the relatively large increase in the thickness of interfacial oxide between HfO_2 and Si substrate.

Fig.3 shows EOT values vs physical thickness of (Tox) HfO_2 layer of Ge and Si MOS devices. We extracted the dielectric constant (k) values for both Ge [fig 3(a)] and Si [fig 3(b)] devices from the slope of the EOT vsTox plots. The obtained dielectric constant of Ge and Si devices of are 19.5 and 8.2 respectively. There is attractive difference in the k values of Ge device showed very high k value relatively when comparing with Si devices. The possible explanation for this significant difference k value might be due to the very thin interfacial layer (native oxide layer) in between HfO_2 and substrate stacks, it is also conformed from the below Fig.3. That the interfacial layer thickness (EOT_i) in Ge device is 0.67nm, whereas the same in Si device is 1.7nm. Hence the effect of low-k interfacial on the dielectric properties of devices is minimized in Ge devices; it is also confirmed by many reports [23]. That the interfacial layer thickness is almost negligible at high-k/Ge stacks, it is an significant property of the Ge MOS device to avoid unnecessary influence of low-k interfacial layer on the electrical properties of MOS devices.

Fig. 4 shows the Current-Voltage (I-V) characteristics of the Ge and Si MOS device at 1MHZ frequencies and 6.0, 8.0 and 10.0 nm thick HfO_2 as-deposited gate dielectric films. It is clear from [fig 4(a)] the dispersion suggests that more bulk oxide traps are present in the films, with the reduction in frequency kinks start appearing in the inversion regions indicate the presence of slow interface states near the valance band [22]. The leakage current in Ge devices [fig. 4(a)] are relatively large when compare with Si devices [fig. 4(b)]. The reason for this observation could the Ge- devices showing large leakage current densities it may be due to the poly crystalline in the HfO_2 films.

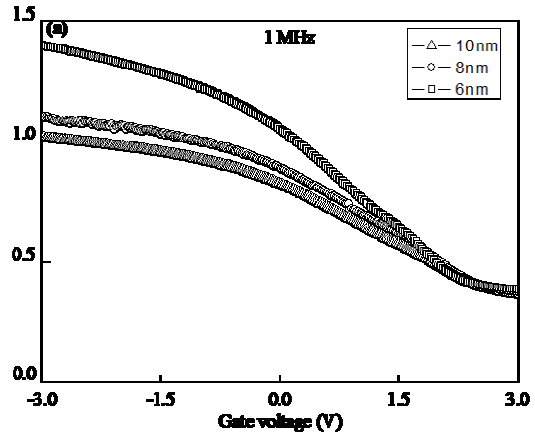

Fig. 2(a)

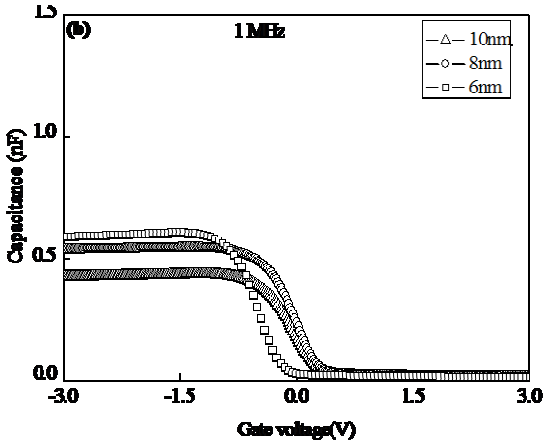

Fig. 2(b)

Fig.2 Capacitance – voltage characteristics of (a) Ge- (b) Si- MOS devices

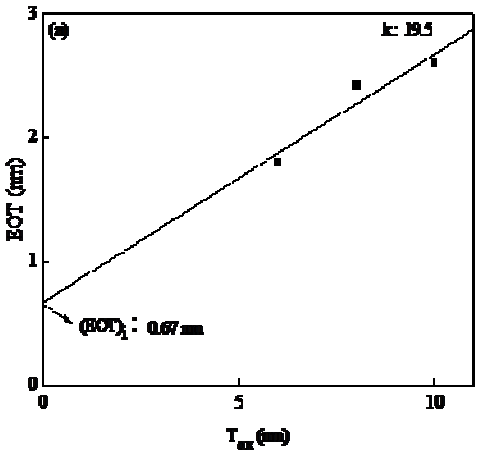

Fig. 3(a)

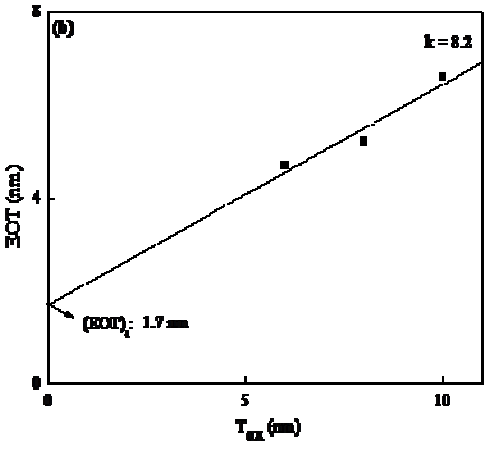

Fig. 3(b)

Fig.3 EOT vs oxide physical thickness (T_{Ox}) of (a) Ge- (b) Si- MOS devices at 1 MHz

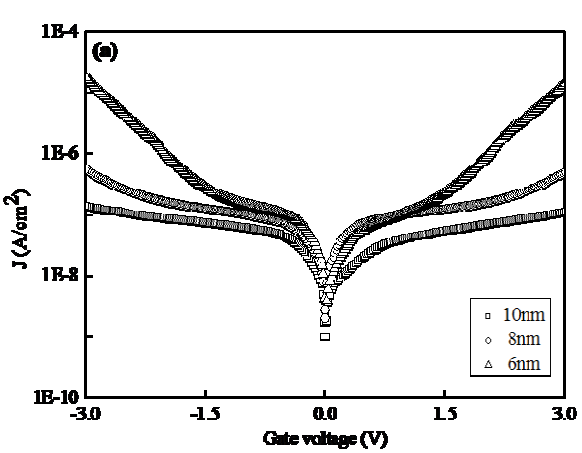

Fig. 4(a)

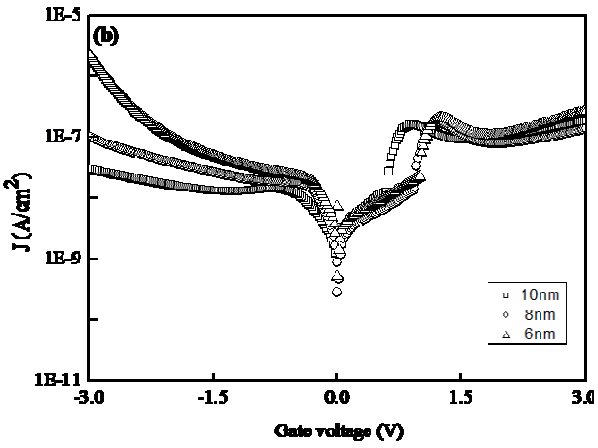

Fig. 4(b)

Fig.4 Current - voltage characteristics of (a) Ge- (b) Si- MOS devices

CONCLUSION

We fabricate the Ge and Si MOS devices using the stacks of Pt/HfO_2 gate stacks and determined their electrical and structural properties. The Si device showed more of a decreased accumulation capacitance due to the significant increase in low-k interfacial oxide thickness compared to Ge device. At the high frequencies the Ge MOS device showed the high dielectric constant than Si MOS device. It could be due to the low interface quality and high interface traps in the Si MOS device. Finally, Ge has been provided solutions for major road blocks that Si technology is facing for advanced CMOS devices due to its higher mobility of both hole and electron.

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