ABSTRACT

Now a day’s industrial applications need high power equipment for conversion of power. At medium voltage applications, to associate one and only power semiconductor switch directly could be a not much productive concept. To conquer this multilevel power converter structure has been presented and concentrated on as an elective in high power and medium voltage applications. Renewable sources like photovoltaic, wind, fuel cells are often handily interfaced to a multilevel converter for high power applications. This paper discussing about PUC converter which is the most advanced topologies of all multilevel converters and having a merit of reduced device count. A comparison is going to be shown for 7, 15, 31 levels of PUC converter with different loads in terms of Total Harmonic Distortion (THD)%. The simulations are performed by using MATLAB/Simulink software.

Key words: Multilevel Converter, Packed U Cell design, THD, Variable Loads

INTRODUCTION

Now a day’s the usage of Multilevel Converters (MLC) are widely used in industry for medium voltage and high power operations. MLC are playing a vital role due to their low harmonic content in output. By varying the switching states of MLC it has various output voltage levels can be produced. In multilevel concept as increasing the voltage levels the THD% in output voltage waveform reduces. Existing concepts of multilevel topologies are following: neutral point-clamped topology (NPC) proposed by Nabae et al. [1]; flying capacitor topology (FC) proposed by Meynard et al. [2]; and classic cascaded H-bridges proposed by Peng et al. [3], in these topologies abounding drawbacks are found if voltage levels are increased. Usually multilevel converter comprises of number of switches, capacitors and DC voltage sources by increasing the voltage level the device count also increased, results in more price and it is difficult in implementation.

So researchers are focused in creating the new ideas in multilevel converters with more benefits in each and every aspect. In existing concepts, such as Cascaded H-bridge topology had more dc voltage sources it may result in the more no of transformers [4]-[8]. So in perspective of all these, a transformer-less converter arrangement is outlined in this paper which is called Packed U Cell (PUC) [9] topology. It accomplishes high power conversion quality by reducing the device count and low switching disturbances with respective to decreased in cost, circuit complexity at higher voltage levels there by avoids in bulky installations compared to existing topologies.

DESIGN AND EVALUATION OF PUC (Packed U Cell) TOPOLOGY

It contains of packed u cells (PUC). Each U cell has an arrangement of two switches and one capacitor. It offers high-energy conversion quality using a small amount of capacitors and power devices, and appropriately they have low production cost. It is very simple in terms of interconnection of components [9]. In this topology number of levels can be recognized by using the following equation:

\[ 2^{n+1} - 1 = \text{Number of levels} \]  \hspace{1cm} \text{where n=1,2,3…}  \hspace{1cm} (1)

No of capacitors can be recognized by using the following equation:

\[ N = 2^{N+1} - 1 \] \hspace{1cm} (2)
where \( N \) is the no of voltage levels, \( N_c \) is the number of capacitors. Similarly the quantity of voltage levels \( N \) with individual to the quantity of switches \( N_{sw} \) given by following equation:

\[
N = 2^{\frac{N_{sw}}{2}} - 1
\]

(3)

In fact, that above equations show the advantages of this topology not only utilizing single DC source but also the reduced number of power switches used to generate the desired voltage levels. For the 7, 15, 31, PUC topology six, eight, ten active switches and two, three, four sources are required compared to the other topologies and the comparison Table 1 give the clear performance of this topology. The main applications of this topology are PV applications, Motor drives etc. It offers better power quality in terms of achievable number of voltage levels, against other multilevel topologies and reliability of this system is more.

**Evaluation of Seven Level**

The output voltage levels are recorded in Table 2. It should be described that \( S_d, S_e \) and \( S_f \) are working in complementary of \( S_a, S_b \) and \( S_c, S_o \) each brace of \( (S_a, S_d), (S_b, S_e) \) and \( (S_c, S_f) \) cannot conduct at the same time. The switching voltage sequence can be given in Table 2. From the table the voltages are as \( V_1, V_1-V_2, V_2, 0, -V_2, V_2-V_1, -V_1 \) and the voltage values are 150 and 50 [10]. Here IGBT switches are used because it is a sort of transistor which works with a greater amount of power transfer and contains a higher switching speed with high efficient. 6IGBT switches are utilized in 7level PUC topology and it can be divided into 2 legs, hence three switches from one leg which is as show in Fig. 1.

### Table 1: Comparison of Various Topologies with PUC Topology

<table>
<thead>
<tr>
<th>Topologies</th>
<th>7-level</th>
<th>15-level</th>
<th>31-level</th>
</tr>
</thead>
<tbody>
<tr>
<td>NPC</td>
<td>Capacitors</td>
<td>Diodes</td>
<td>Switches</td>
</tr>
<tr>
<td>FC</td>
<td>6</td>
<td>10</td>
<td>12</td>
</tr>
<tr>
<td>CHB</td>
<td>3</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>HCHB</td>
<td>2</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>PUC</td>
<td>2</td>
<td>0</td>
<td>6</td>
</tr>
</tbody>
</table>

![Fig.1.Seven level converter](image1.png)

![Fig.2.Fifteen level converter](image2.png)
Evaluation of Fifteen Level

Table 3 shows the switching sequence of the fifteen level operation in case of $V_1 = 3$ and $V_2 = 7$ and design is shown in Fig. 2. Switches $S_a$ and $S_b$ are operated complimentary, but only $S_a, S_b, S_c, S_d$ switch is considered in table. Here we have taken the values as $V_1=420V, V_2=180V$ and $V_3=60V$ [11].

Evaluation of Thirty-One Level

The switching Table 4 shows the analysis of switching operation for thirty-one level and Fig. 3 shows the topology of 31 level inverter. The pure sinusoidal waveform can be obtained by increasing the voltage levels hence the input voltages are [12]

$$V_1 = V_{dc}, V_2 = V_{dc} \frac{7}{15}, V_3 = V_{dc} \frac{3}{15}, V_4 = V_{dc} \frac{1}{15}$$
RESULTS AND DISCUSSION

Simulation of seven, fifteen, thirty-one levels of multilevel inverter at R, RL, RLC, Motor loads are performed by using matlab software and the comparison for Total Harmonic Distortion of voltage and current is shown for every loads at each level are performed.

Analysis of Seven Level Inverter

![Graphs showing voltage and current for R, RL, RLC loads](image-url)
Fig. 6. Output voltage current for Seven level RLC-load

Fig. 7. Output voltage current for Seven Level Motor-load
Analysis of Fifteen Level Inverter

Fig. 8. Output voltage current for Fifteen level R-load

Fig. 9. Output voltage current for Fifteen level RL-load
Fig. 10. Output voltage current for Fifteen level RLC-load

Fig. 11. Output voltage current for Fifteen level Motor-load
Analysis of Thirty-one Level Inverter

Fig. 12. Output voltage current for Thirty-one level R-load

Fig. 13. Output voltage current for Thirty-one level RL-load
Fig. 14. Output voltage current for Thirty-one level RLC-load

Fig. 15. Output voltage current for Thirty-one level Motor-load
Harmonic Analysis multilevel PUC Inverter at different Levels

The following graphs show the THD comparisons for 7, 15 and 31 levels at various loads are analyzed and which is as shown in the graphical representation for each level. Hence by increasing the levels the THD percentage reduces which is as shown in the graphs Fig 16-18.
Table 4 Comparison for Various Loads and Levels in terms of THD%  

<table>
<thead>
<tr>
<th>Variable Loads</th>
<th>Total Harmonic Distortion %</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>7-level</td>
</tr>
<tr>
<td>RL</td>
<td>V 16.90</td>
</tr>
<tr>
<td>RLC</td>
<td>V 16.90</td>
</tr>
<tr>
<td>MOTOR</td>
<td>V 16.90</td>
</tr>
</tbody>
</table>

CONCLUSION

The simulation of PUC (Packed U Cell) topology is performed for 7,15,31 levels at variable loads of R, RL, RLC & Motor using MATLAB/SIMULINK software. When the load is resistive, the %THD for 7,15,31 levels of output voltages are found to be 16.89%, 13.30%, 12.43%. In the cases of RL, RLC & Motor loads the %THD found be same at each load 16.90%, 13.31%, 12.44% respectively for output voltage and also for output current they are found to be 5.60%, 5.54%, 4.69% at RL-load, 5.49%, 5.39%, 4.45% at RLC-load, and 6.08%, 5.83%, 5.71% at Motor load respectively Table 4. The FFT analysis of each load case is fulfilled through graphical representation. It is evident that as the output voltage levels increases the %THD gets reduced. The figure of merit of this topology is reduction in the number of switches as level increases. Hence, it reduces the cost of implementation besides topology complexity compared to other existing topologies such as Neutral Point Clamping, Flying Capacitor, Cascaded H-Bridge and Hybrid Cascaded H-Bridge.

REFERENCES